REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Upon entry of this amendment, claims 1-81 and newly added claims 82-115 will remain in the application.

Double patenting rejections

Claims 1 to 59 and 76 to 81 were rejected under the judicially created doctrine of obviousness-type double patenting as allegedly being unpatentable over claims 1-31 of U.S. Patent No. 5,700,333 to Yamazaki et al. ("the '333 patent").

The Action states that "in the absence of unobvious results, it would have been obvious for one of ordinary skill in the art to determine through routine experimentation the optimum, operable device formed as the instant claims form any device and heating in order to decrease heating time."

The Action is using an "obvious to try" rationale to reject the claims. Applicants respectfully traverse the rejections.

> "*[O]bivious to try* is not the standard of 35 USC 103… Disregard for the unobviousness of the results of 'obvious to try' experiments disregards the 'invention as a whole' concept of § 103…" (emphasis in original) *In re Antonie*, 559 F.2d 618, 195 USPQ 6, 8 (CCPA 1977) (citations omitted) cited by I*n re O'Farrell*, 853 F.2d 894, 903 , 7 USPQ2d 1673, 1681 (Fed. Cir. 1988), MPEP 2145.X.B.

The claims recite numerous limitations not found in the claims of the '333 patent.

Consider exemplary claim 1, which recites the limitations:

> "...wherein the first and second portions of the crystalline semiconductor film are in contact with the insulating surface over the substrate;
> performing a second heat treatment so that the element contained in the second portion is moved to the first portion in a direction parallel to the insulating surface; and
> patterning the crystallized semiconductor film to form a crystalline semiconductor island in the second portion thereby removing the first portion of the crystalline semiconductor film;..." (emphasis added)

None of these limitations are recited in the claims of the '333 patent. Furthermore, the '333 patent provides no teaching, suggestion, or motivation to pursue these limitations through experimentation. Accordingly, Applicants submit that the Action fails to make a *prima facie* case of obviousness-type double patenting.

Section 103 rejections

Claims 1-16, 76, and 77 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over the '333 patent.

The Action again uses an obvious to try rationale to reject the claims. Applicants submit that the Action fails to make a *prima facie* case of obviousness for the reasons stated above.

Furthermore, Applicants submit that the recited method has several advantages over the method disclosed in the '333 patent.

In the '333 patent, it appears that the crystallization promoting element is moved in a direction perpendicular to a substrate, that is, in a direction toward the upper portion of the crystalline semiconductor film. If the gettering process suggested in column 6 of the '333 patent was applied to a thin film transistor (TFT) manufacturing process, the interface characteristic between the semiconductor film and the gate insulating film would decrease because it is difficult to remove only the upper portion of the semiconductor film smoothly. As a result, the surface of the semiconductor film would be rough. On the other hand, the gettering process taught by Applicants proceeds in a direction parallel (lateral) to the insulating surface, and hence there is no roughening effect to the surface of the semiconductor film. Thus, the gettering process taught by Applicants may advantageously improve in the interface characteristic of the TFT.

For the reasons stated above, Applicants submit that the claims are allowable over the '333 patent.

Claims 17-59, 75 and 78-81 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over the '333 patent in view of Zhang et al (US 5,569,936).

Zhang et al is merely cited for its disclosure of using lasers to crystallize amorphous silicon.

For the reasons stated above, Applicants submit that the claims are allowable over the '333 patent in view of Zhang et al.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be allowed. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Version with markings to show changes made

In the claims:

Claims 82-115 have been added.

Claims 1, 3, 5, 9, 11, 13, 17, 19, 21, 25, 27, 29, 33, 36, 39, 42, 45, 46, 49, 52, 53, 57, and 76-81 have been amended as follows:

1. (Amended) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film comprising silicon over a substrate having an insulating surface;

[introducing into] providing the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film by a first heat treatment to form a crystalline semiconductor film;

introducing an impurity element belonging to Group 15 into a first portion of the crystalline semiconductor film while a second portion of the crystalline semiconductor film is not [introduced] provided with the impurity element;

wherein the first and second portions of the crystalline semiconductor film are in contact with [a same] the insulating surface over the substrate;

[gettering the element which promotes crystallization by a second heat treatment to the first portion of the crystallized semiconductor film] performing a second heat treatment so that the element contained in the second portion is moved to the first portion in a direction parallel to the insulating surface; and

patterning the crystallized semiconductor film to form a crystalline semiconductor island in the second portion thereby removing the first portion of the crystalline semiconductor film;

forming an active layer of the thin film transistor using the crystalline semiconductor island,

wherein the second heat treatment [during gettering the element] is performed in a temperature range not exceeding a glass transition point of the substrate.

3. (Amended) A method according to claim 1, wherein the second heat treatment [during gettering] is performed in the temperature range from 500 to 700°C.

5. (Amended) A method according to claim 1, wherein the second heat treatment [during gettering] is furnace annealing.

9. (Amended) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film comprising silicon over a substrate having an insulating surface;

selectively [introducing into] providing a first portion of the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film by a first heat treatment to form a crystalline semiconductor film, so that a crystallization proceeds from the first portion in a lateral direction to the insulating surface;

introducing an impurity element belonging to Group 15 into a second portion of the crystalline semiconductor film while a third portion of the crystalline semiconductor film is not [introduced] provided with the impurity element;

wherein the second and third portions of the crystalline semiconductor film are in contact with [a same] the insulating surface over the substrate;

[gettering the element second portion of the crystalline semiconductor film] performing a second heat treatment so that the element contained in the third portion is moved to the second portion in a lateral direction to the insulating surface; and

patterning the crystalline semiconductor film to form a crystalline semiconductor island in the third portion thereby removing the second portion of the crystalline semiconductor film;

forming an active layer of the thin film transistor using the crystalline semiconductor island,

wherein the second heat treatment [during gettering the element] is performed in a temperature range not exceeding a glass transition point of the substrate.

11. (Amended) A method according to claim 9, wherein the second heat treatment [during gettering the element] is performed in the temperature range from 500 to 700°C.

13. (Amended) A method according to claim 9, wherein the second heat treatment [during gettering] is furnace annealing.

17. (Amended) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film comprising silicon over a substrate having an insulating surface;

[introducing into] providing the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film by a first heat treatment to form a crystalline semiconductor film;

irradiating a laser light or an intense light to the crystalline semiconductor film;

introducing an impurity element belonging to Group 15 into a first portion of the crystalline semiconductor film after the irradiating step, while a second portion of the crystalline semiconductor film is not [introduced] provided with the impurity element;

wherein the first and second portions of the crystalline semiconductor film are in contact with [a same] the insulating surface over the substrate;

[gettering the element by a second heat treatment to the first portion of the crystalline semiconductor film] performing a second heat treatment so that the element contained

in the second portion is moved to the first portion in a lateral direction to the insulating surface;

patterning the crystalline semiconductor film to form a crystalline semiconductor island in the second portion thereby removing the second portion of the crystalline semiconductor film;

forming an active layer of the thin film transistor using the crystalline semiconductor island,

wherein the second heat treatment [during gettering] is performed in a temperature range not exceeding a glass transition point of the substrate.

19. (Amended) A method according to claim 17, wherein the second heat treatment [during gettering] is performed in the temperature range from 500 to 700°C.

21. (Amended) A method according to claim 17, wherein the second heat treatment [during gettering] is furnace annealing.

25. (Amended) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film comprising silicon over a substrate having an insulating surface;

selectively [introducing into] providing a first portion of the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film by a first heat treatment to form a crystalline semiconductor film, so that a crystallization proceeds from the first portion of the amorphous semiconductor film in a lateral direction to the insulating surface;

irradiating a laser light or an intense light to the crystalline semiconductor film;

introducing an impurity element belonging to Group 15 into a second portion of the crystalline semiconductor film after the irradiating step, while a third portion of the crystalline semiconductor film is not introduced with the impurity element;

wherein the second and third portions of the crystalline semiconductor film are in contact with [a same] the insulating surface over the substrate;

[gettering the element by a second heat treatment to the second portion of the crystalline semiconductor film]

performing a second heat treatment so that the element contained in the third portion is moved to the second portion in a lateral direction to the insulating surface;

patterning the crystalline semiconductor film to form a crystalline semiconductor island in the third portion thereby removing the second portion of the crystalline semiconductor film;

forming an active layer of the thin film transistor using the crystalline semiconductor island,

wherein the second heat treatment [during gettering] is performed in the temperature range not exceeding a glass transition point of the substrate.

27. (Amended) A method according to claim 25, wherein the second heat treatment [during gettering] is performed in the temperature range from 500 to 700°C.

29. (Amended) A method according to claim 25, wherein the second heat treatment [during gettering] is furnace annealing.

33. (Amended) A method according to claim 1, wherein said step of introducing [an] the impurity element belonging to Group 15 is performed by plasma doping.

36. (Amended) A method according to claim 9, wherein said step of introducing [an] the impurity element belonging to Group 15 is performed by plasma doping.

39. (Amended) A method according to claim 17, wherein said step of introducing [an] the impurity element belonging to Group 15 is performed by plasma doping.

42. (Amended) A method according to claim 25, wherein said step of introducing [an] the impurity element belonging to Group 15 is performed by plasma doping.

45. (Amended) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film comprising silicon over a substrate having an insulating surface;

[introducing into] providing the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film by a first heat treatment to form a crystalline semiconductor film;

introducing an impurity element belonging to Group 15 into a first portion of the crystalline semiconductor film while a second portion of the crystalline semiconductor film is not [introduced] provided with the impurity element;

wherein the first and second portions of the crystalline semiconductor film are in contact with [a same] the insulating surface over the substrate;

[gettering the element which promotes crystallization by a second heat treatment into the first portion of the crystalline semiconductor film] performing a second heat treatment so that the element contained in the second portion is moved to the first portion in a lateral direction to the insulating surface;

patterning the crystalline semiconductor film to form a crystalline semiconductor island in the second portion thereby removing the first portion of the crystalline semiconductor film;

forming a gate insulating film over the crystalline semiconductor island;

forming at least one gate electrode comprising a metal on the gate insulating film;

doping an impurity element into at least a second portion of the crystalline semiconductor island to form a lightly doped drain region; and

forming at least a source region and a drain region by doping an impurity element into third portions of the crystalline semiconductor island,

wherein the second heat treatment [during gettering] is performed in a temperature range not exceeding a glass transition point of the substrate.

46. (Amended) A method according to claim 45, wherein the second heat treatment [during gettering] is performed in the temperature range from 500 to 700°C.

49. (Amended) A method according to claim 45, wherein said step of introducing [an] the impurity element belonging to Group 15 is performed by plasma doping.

52. (Amended) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film comprising silicon over a substrate having an insulating surface;

[introducing into] providing the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film by a first heat treatment to form a crystalline semiconductor film;

introducing an impurity element belonging to Group 15 into a first portion of the crystalline semiconductor film while a second portion of the crystalline semiconductor film is not [introduced] provided with the impurity element;

[gettering the element by a second heat treatment into the first portion of the crystalline semiconductor film] performing a second heat treatment so that the element contained in the second portion is moved to the first portion in a lateral direction to the insulating surface;

patterning the crystalline semiconductor film to form a crystalline semiconductor island in the second portion thereby removing the first portion of the crystalline semiconductor film;

forming a gate insulating film over the crystalline semiconductor island;

forming at least one gate electrode comprising a metal on the gate insulating film;

doping an impurity element into at least a second portion of the crystalline semiconductor island to form a lightly doped drain region;

forming at least a source region and a drain region by doping an impurity element into third portions of the crystalline semiconductor island;

forming an interlayer insulating film comprising silicon over the gate electrode;

forming an interlayer insulating film comprising an organic resin film over the interlayer insulating film; and

forming a pixel electrode that is electrically connected to the source region or drain region through a contact hole over the interlayer film;

wherein the second heat treatment [during gettering] is performed in a temperature range not exceeding a glass transition point of the substrate.

53. (Amended) A method according to claim 52, wherein the second heat treatment [during gettering] is performed in the temperature range from 500 to 700°C.

57. (Amended) A method according to claim 52, wherein said step of introducing [an] the impurity element belonging to Group 15 is performed by plasma doping.

76. (Amended) A method according to claim 1, wherein the element in the crystalline semiconductor island after the [gettering step] second heat treatment has a concentration in a range of 1×10^{18} atoms/cm^3 or lower.

77. (Amended) A method according to claim 9, wherein the element in the crystalline semiconductor island after the [gettering step] second heat treatment has a concentration in a range of 1×10^{18} atoms/cm^3 or lower.

78. (Amended) A method according to claim 17, wherein the element in the crystalline semiconductor island after the [gettering step] second heat treatment has a concentration in a range of 1×10^{18} atoms/cm^3 or lower.

79. (Amended) A method according to claim 25, wherein the element in the crystalline semiconductor island after the [gettering step] second heat treatment has a concentration in a range of 1×10^{18} atoms/cm^3 or lower.

80. (Amended) A method according to claim 45, wherein the element in the crystalline semiconductor island after the [gettering step] second heat treatment has a concentration in a range of 1×10^{18} atoms/cm^3 or lower.

81. (Amended) A method according to claim 52, wherein the element in the crystalline semiconductor island after the [gettering step] second heat treatment has a concentration in a range of 1×10^{18} atoms/cm^3 or lower.